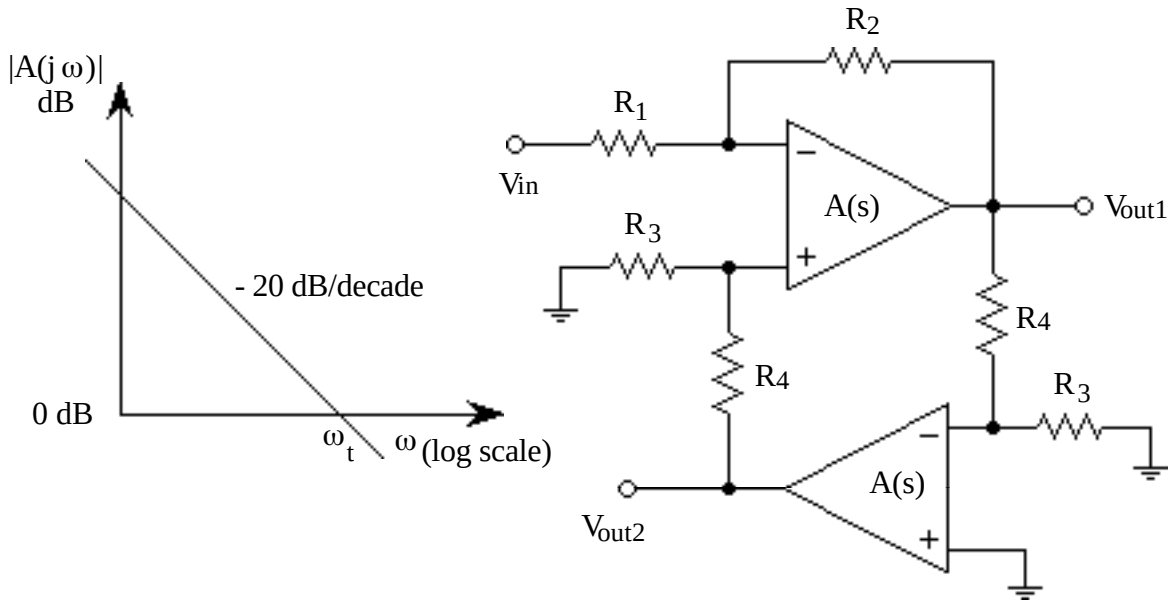
TOPIC: Linear Circuits (ENEL343)

Q.1 The circuit shown below is a second-order filter containing no capacitor external to the op amps (it is called an active-R biquad). Assume that the two op amps are identical with infinite input resistance, zero output resistance and open-loop gain A(s) as given by the Bode plot shown below.

(a) Obtain the transfer functions $\frac{V_{out1}}{V_{in}}(s)$ in terms of R's and ω_t.

(b) Obtain expressions for ω_o and Q and their sensitivities with respect to R's and ω_t.

(c) Use this circuit to realize a second-order bandpass filter with unity center-frequency gain, center frequency of 10 krad/sec and a BW of 1 krad/sec. Assume that the op amps have unity-gain-bandwidth (ω_t) of 10 Mrad/sec. Obtain all the resistors values.



Q.2 (a) Using Mesh analysis write by <u>inspection</u> a set of mesh matrix equations (size 2 x 2) in the form [**A][I]** = **V** for the circuit shown in Figure 2. Your final answer should contains numbers only in the **A** matrix and the **V** column vector.

(b) Using the result in part (a) solve the voltage *v* across the 4 Ω resistor.

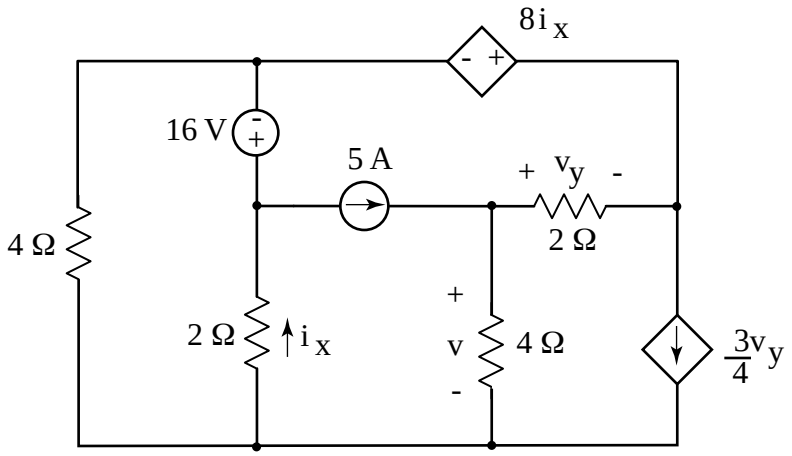


Figure 2

Q.3 (a) Using any method of your choice determine the steady state current $i_{out}(t)$ in the circuit shown in Figure 3 if $v_s(t) = 12\cos(2t + 45^\circ)$ V.

(b) Determine the natural response of this circuit assuming the capacitor held an initial voltage of $v_c(0^-) = V_0$ and the initial current through the inductor $i_L(0^-) = I_0$, respectively.

(c) If $I_o = -1A$ and $V_o = 2V$, plot $i_{out}(t)$ versus time.

(d) Plot the asymptotic frequency response of this circuit if i_{out} is considered the output of the circuit and the independent source as the input.

(e) If i_{out} is considered the output of the circuit and the independent source as the input, is this circuit reciprocal? Give a brief explanation for your reasoning.

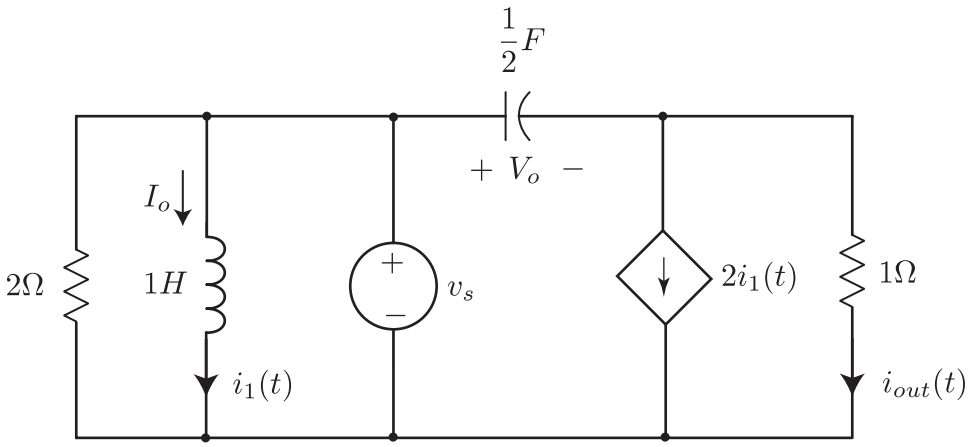


Figure 3

TOPIC: Digital Ciruits (ENCM467)

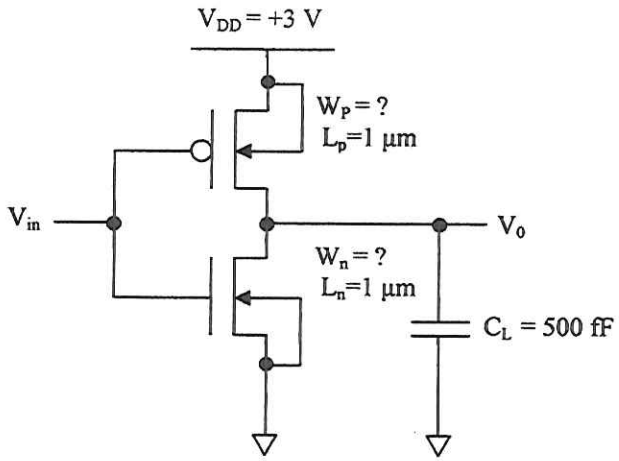
Q.1 Design a static CMOS inverter (see figure 2), using 1μm long nMOS and pMOS transistors and of appropriate widths, so as to meets the following performance requirements:

1) A falling delay of 0.2 ns, for an output transition from 2 V to 0.6 V, assuming an output load capacitance of 500 fF and ideal step input of 3V being applied to the inverter.
2) An inverter switching threshold voltage $V_{INV} = 1.4\,\text{V}$.

2μm CMOS device and process parameters

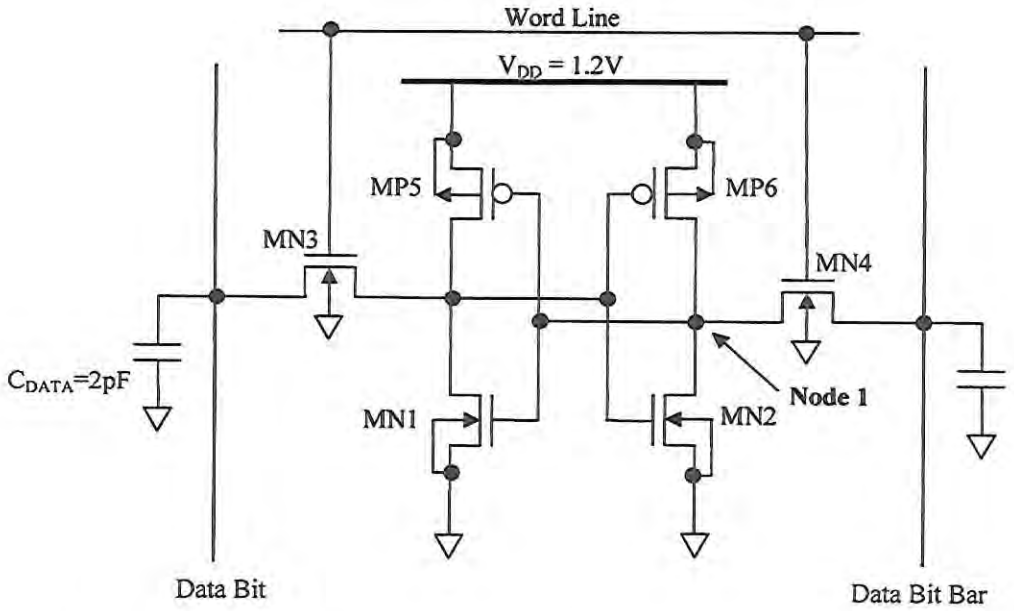
$k_n' = 100\ \mu\text{A.V}^{-2};\ V_{T0(n)} = 0.8\,\text{V};\ L_n = 1\,\mu m\ ;W_{n(\min)} = 2\,\mu m\ ;\ \gamma_n = 0.4\ \text{V}^{0.5};\ |2\phi_{F(n)}| = 0.6\,\text{V}$

$k_p' = 50\ \mu\text{A.V}^{-2};\ V_{T0(p)} = -1.0\,\text{V};\ L_p = 1\,\mu m\ ;W_{p(\min)} = 2\,\mu m;\ \gamma_p = 0.4\ \text{V}^{0.5};\ |2\phi_{F(p)}| = 0.6\,\text{V}$



Q.2 What are the respective widths of transistors MN4 and MP6 of the CMOS static memory cell shown below, so that the design meets the following requirements:

(a) The voltage at **node 1** during the **WRITE '1'** operation must be pulled down to at least **0.4 V.**

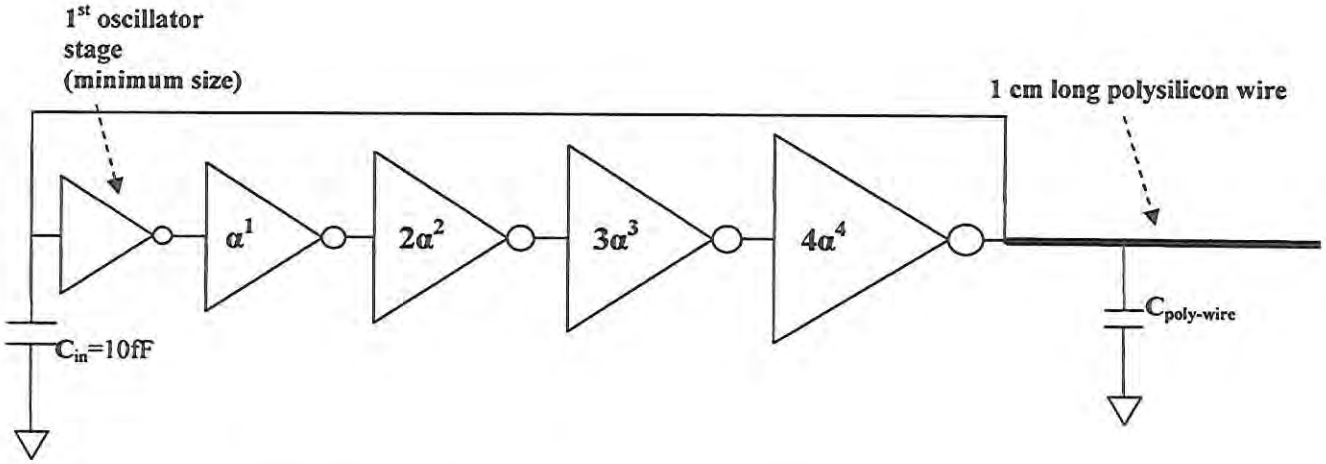


$k_p' = 130\ \mu A.V^2$; $k_n' = 400\ \mu A.V^2$; $V_{T0(n)} = 0.4\ V$; $V_{T0(p)} = -0.4\ V$; $\gamma_n = 0.2V^{1/2}$; $\gamma_p = 0.2V^{1/2}$
$|2\phi_F| = 0.88V$; $L_{MN1} = L_{MN2} = L_{MN3} = L_{MN4} = L_{MP5} = L_{MP6} = 0.1\mu m$;

Q.3 In order to generate an on-chip clock, a tapered a five stage ring oscillator is used in order to drive a long capacitive polysilicon wire, as shown below. The first ring oscillator stage is a minimum sized inverter with C_{in} = 10fF, and a propagation delay of 175 pS, when driving a similar minimum sized inverter. The sizes of the 2nd and subsequent stages are scaled by α, $2\alpha^2$, $3\alpha^3$, $4\alpha^4$ respectively. Given that that polysilicon line width is 5μm with a per unit area capacitance of 0.05 fF/μm^2

a). Determine the optimum scaling factor (α) of the ring oscillator stages in order minimize the propagation delay.

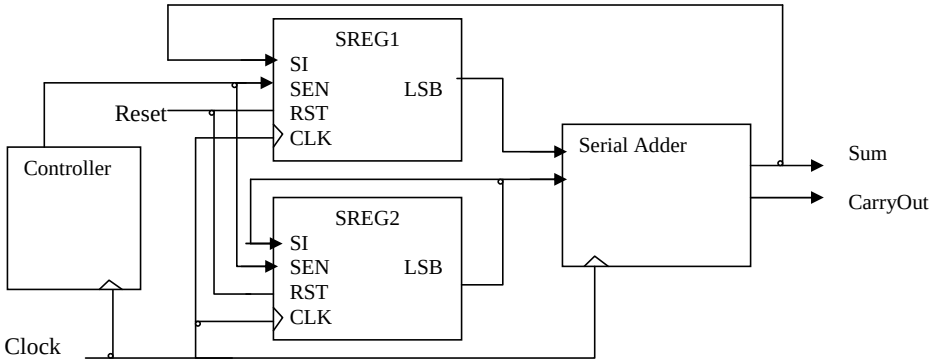
b). What is the frequency of oscillation of the tapered ring oscillator?



A 5 stage tapered ring oscillator driving a polysilicon wire

Q.1 (parts a-c on following pages)

Consider the serial adder below. Two shift registers $SREG1$ and $SREG2$ are used to hold the four bit numbers to be added. Each register has a Shift Enable signal SEN, serial input SI, Clock and Reset. When $SEN = 1$ and the Clock is pulsed, SI is entered into the Most significant bit, MSB, of the register, as the contents of the register are shifted right one position. The connections needed for initial loading of the registers are not shown. The upper register serves as accumulator, and after four shifts its contents is replaced with the sum of the initial numbers. The lower register is connected as a cyclic shift registers, so after four shifts it is back to its original state and the second number is not lost.



(a) [Design the Serial Adder block for the circuit above. It should include a full adder and a flip-flop to store carry, to be used at the next clock cycle. At each clock cycle, one pair of bits is added in the full adder. It should also include a logic which must accommodate the following operation involving Clock and the SEN signal: when SEN is 1, the carry bit is stored in the carry flip-flop on the clock edge.

(b) Design the Controller (based on a Mealy FSM) so that after receiving a start signal, N, it will output $SEN = 1$ for four clocks and then stop. $SEN = 1$ shifts the sum bit into the upper register and causes the lower register to rotate right. Draw the state graph and the state table. Assume that the start signal N is terminated before the network returns to the first state, so no further action occurs until another start signal is received. Once the second state is reached, the network operation continues regardless of the value of N.

(c) Provide an alternative high-level FSM for the FSM in part (b).

Q.2 (parts a-d on this and following pages)

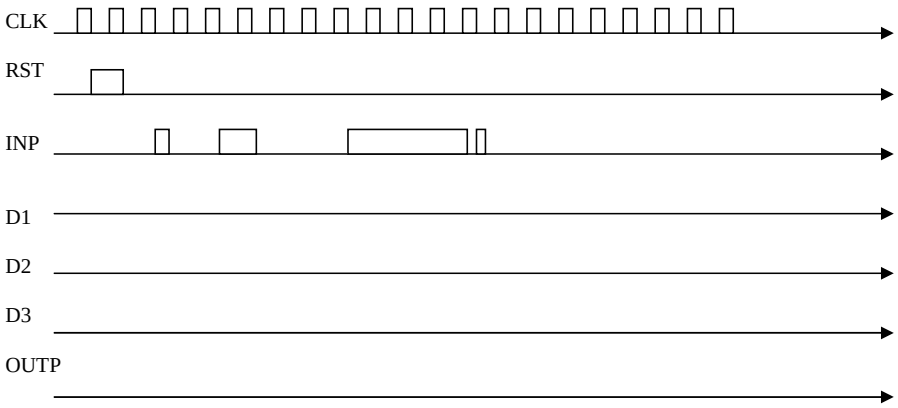
Consider the VHDL code that defines a debounce circuit, which can be used to qualify the input of a push-button switch.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity DEBOUNCE is
    port(INP, RST, CLK: in std_logic;
         OUTP: out std_logic;
end entity DEBOUNCE;

architecture BEHAV of DEBOUNCE is
 signal D1, D2, D3:  std_logic;
 begin
  process (CLK, RST)
  begin
    if (RST = '1') then
       D1 <= '0';
      D2 <= '0';
      D3 <= '0';
    elsif (CLK'event and CLK = '1') then
      D1 <= INP;
      D2 <= D1;
      D3 <= D2;);
     end if;
  end process;
      OUTP <= D1 and D2 and (not D3);
end architecture BEHAV;
```

(a) Draw the circuit and its timing diagram (see the template below) to answer the question: why this circuit is called a debounce circuit?



(b) In addition, the circuit ensures that the output indicating the button press is of fixed duration regardless of how long the actual button is pressed. How long is this fixed duration?

(c) Propose an alternative debounce circuit solution, based on a counter (draw the design schematics). Specify the counter size.

(d) Provide the VHDL fragment corresponding to the debouncer based on the counter from part (c) in the space provided below.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity DEBOUNCE1 is
    port


end entity DEBOUNCE1;
architecture BEHAV of DEBOUNCE1 is









end architecture BEHAV;
```

Field of Study Examination, Feb 24 2017

Subject area: Circuits and Electronics

This question paper has 7 pages (not including this cover page).

This question paper has 6 questions.

Answer a minimum of one question and at most three questions from this subject area.

Use a separate booklet (i.e., blue booklet) for the answers to questions in this subject area.

1. This question has 7 parts (a)-(g).

   (a) Draw a circuit diagram of a CMOS inverter.

   (b) Assume that $\mu_n = 3\mu_p$, $V_{dd} = 1.8\ V$, $V_{tn} = |V_{tp}| = 0.5\ V$, $\lambda = 0.1$, and the width of NMOS is 1 μm. Explain how you would select the size of the PMOS transistors such the threshold voltage of the inverter was 1 V?

   (c) What are the V_{OH} and V_{OL} of the inverter designed in (b)

   (d) What capacitance does this inverter present to a preceding logical gate? Show your answer in terms of the small signal transistor capacitances.

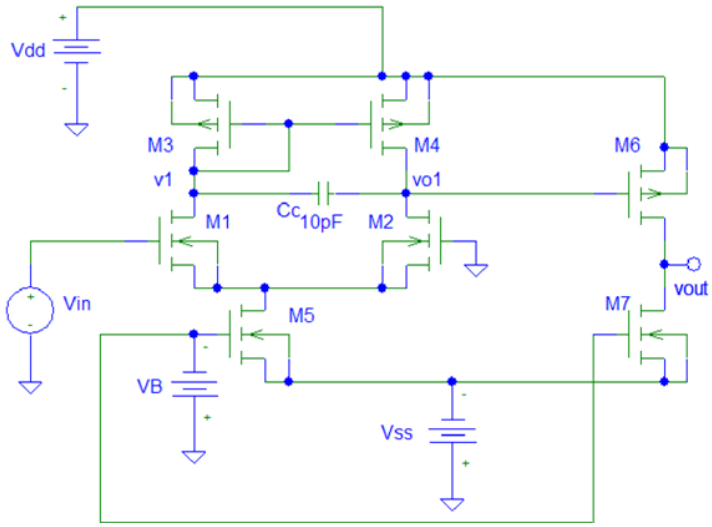
   (e) What is the output capacitance of this inverter? Show your answer in terms of the small signal transistor capacitances.

   (f) What transistor width ratios would you select to make t_{pHL} equal to t_{pLH}?

   (g) What transistor width ratios would you select to minimize the average time delay (t_p)?

2. This question has 3 parts (a)-(c).

A CMOS 2-stage OTA is shown below



$g_{m1,2} = 0.581\,mA/V,\ g_{ds1,2} = 0$

$g_{m3,4} = 0.75\,mA/V,\ g_{ds3,4} = 8.5\,\mu A/V$

$g_{m5} = 1.13\,mA/V,\ g_{ds5} = 0$

$g_{m6} = 2.64\,mA/V,\ g_{ds6} = 27.4\,\mu A/V$

$g_{m7} = 2\,mA/V,\ g_{ds7} = 23.8\,\mu A/V$

The layout engineer has inadvertently connected the compensation capacitor as shown, instead of connecting it between the gate and drain of M6.

(a) Derive an analytic expression for the gain v_{o1}/v_{in} of the circuit **formed by transistors M1 to M5** (that is, from the input to the gate of M6), in terms of the small-signal parameters. Be sure to include C_c in your calculations, and arrange your answer in a form that will allow you to sketch a Bode gain magnitude graph. Note that $g_{ds1} = g_{ds2} = g_{ds5} = 0$, so do not use them. Also, assume that the small-signal conductance of the diode-connected transistor M3 is approximately g_{m3}.

(b) Calculate the gain of the gain stage formed by M6 and M7. (Numerical value).

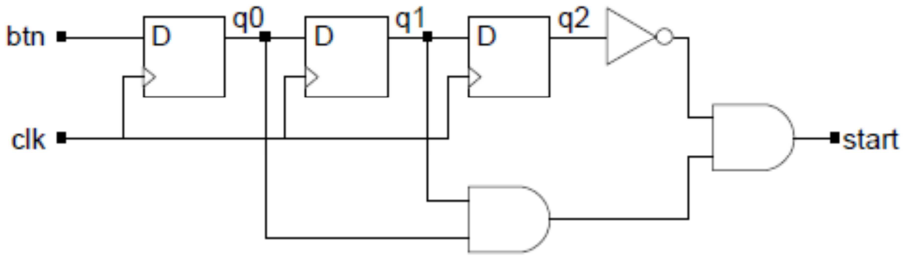
(c) Plot the Bode gain magnitude response of the overall amplifier gain v_{out}/v_{in} in dB, showing all important features.

3. Design a BJT differential amplifier that provides two single-ended outputs (at the collectors). The amplifier is to have a differential gain (to each of the two outputs) of at least 100 V/V, a differential input resistance $\geq$10 kΩ, and a common-mode gain (to each of the two outputs) no greater than 0.1 V/V. Use a 2-mA current source for biasing. Give the complete circuit with component values and suitable power supplies that allow for $\pm$2 V swing at each collector. Specify the minimum value that the output resistance of the bias current source must have. The BJTs available have $\beta \geq$100. What is the value of the input common-mode resistance when the bias source has the lowest acceptable resistance?

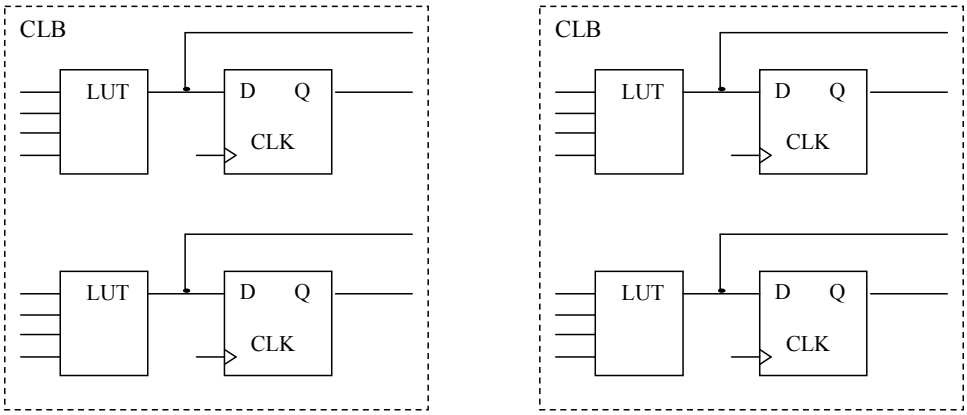
4. An npn BJT with grounded emitter is operated with $V_{BE} = 0.700$ V, at which the collector current is 1 mA. A 10-kΩ resistor connects the collector to a +15 V supply. What is the resulting collector voltage V_C? Now, if a signal applied to the base raises v_{BE} to 705 mV, find the resulting total collector current i_C and total collector voltage v_C using the exponential $i_C - v_{BE}$ relationship. For this situation, what are v_{be} and v_c? Calculate the voltage gain v_c/v_{be}. Compare with the value obtained using the small-signal approximation, that is, $-g_m R_C$.

5. This question has 3 parts (a)-(c). **Note that this question also appears in the Computer Engineering exam. If you attempt this question, it will only count once, towards whichever exam you attempt it in.**

(a) Consider the circuit below.



Consider implementing the circuit on an FPGA. Create a sketch of such implementation using the two CLBs shown below.



(b) Show the content (the function truth tables) of the used LUTs.

(c) Create an FSM based on the circuit in (a). Assume that reset resets to the first state. Derive the excitation and output equations.

6. This question has 2 parts (a)-(b). Part (a) has 2 subparts (i)-(ii) and part (b) has 3 subparts (i)-(iii).

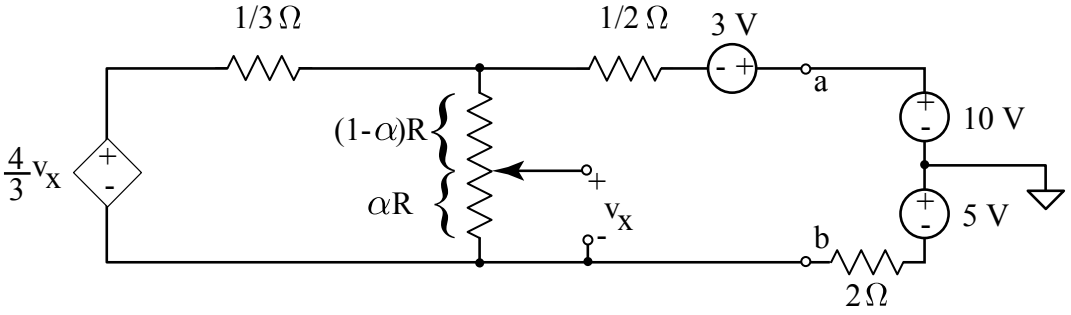
(a) Consider the circuit shown below. It contains a potentiometer modeled by two variable resistors of value αR and $(1-\alpha)R$ where α is a variable $0 \leq \alpha \leq 1$ and $R = 3\ \Omega$. For the circuit, do the following:

i. Find the Thevenin equivalent of the circuit to the left of the nodes a-b.

ii. Determine the value of α for

A. $R_{TH} = -1\ \Omega$

B. $R_{TH} = 1\ \Omega$



(b) The network shown in the figure below has been in that state for a long time with the switches closed. At $t = 0$, the switches are simultaneously opened as indicated by the arrows. For this circuit using Laplace Transform techniques do the following;

i. Determine the poles of this circuit for $t \geq 0$.

ii. Determine the current $i_c(t)$ through the capacitor for $t \geq 0$.

iii. Using the final value theorem determine $v_{4\Omega}(\infty)$.

Tables of Laplace Transforms are given on the page following.

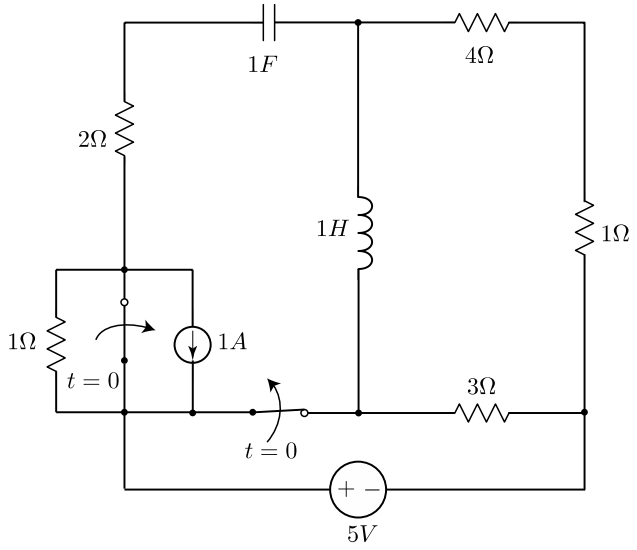


Table of Laplace Transforms

$f(t)$ for $t \geq 0$	$\mathcal{L}(s)$
$u(t)$	$\frac{1}{s}$
$e^{-at}u(t)$	$\frac{1}{s+a}$
$t^n u(t)$	$\frac{n!}{s^{n+1}}$ $(n = 0, 1, ..)$
$\sin(\omega t)u(t)$	$\frac{\omega}{s^2+\omega^2}$
$\cos(\omega t)u(t)$	$\frac{s}{s^2+\omega^2}$
$e^{-at}\sin(\omega t)u(t)$	$\frac{\omega}{(s+a)^2+\omega^2}$
$e^{-at}\cos(\omega t)u(t)$	$\frac{s+a}{(s+a)^2+\omega^2}$
$e^{-at}\left[C\cos(\omega t) + \frac{D-aC}{\omega}\sin(\omega t)\right]u(t)$	$\frac{Cs+D}{(s+a)^2+\omega^2}$