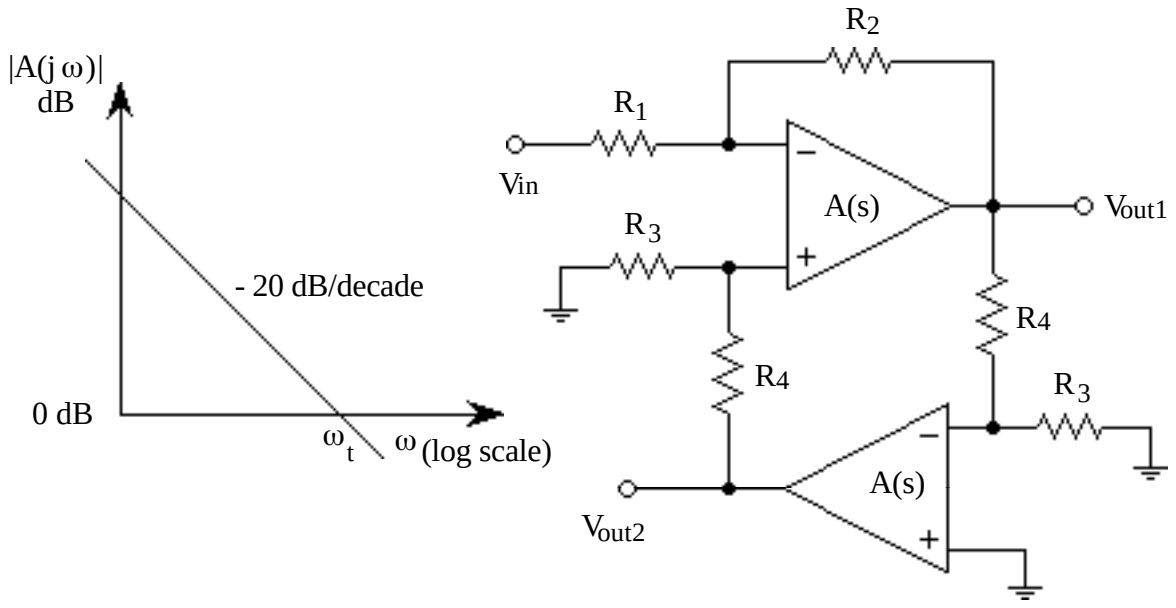
TOPIC: Linear Circuits (ENEL343)

Q.1 The circuit shown below is a second-order filter containing no capacitor external to the op amps (it is called an active-R biquad). Assume that the two op amps are identical with infinite input resistance, zero output resistance and open-loop gain A(s) as given by the Bode plot shown below.

(a) Obtain the transfer functions $\frac{V_{out1}}{V_{in}}(s)$ in terms of R's and ω_t.

(b) Obtain expressions for ω_o and Q and their sensitivities with respect to R's and ω_t.

(c) Use this circuit to realize a second-order bandpass filter with unity center-frequency gain, center frequency of 10 krad/sec and a BW of 1 krad/sec. Assume that the op amps have unity-gain-bandwidth (ω_t) of 10 Mrad/sec. Obtain all the resistors values.



Q.2 (a) Using Mesh analysis write by <u>inspection</u> a set of mesh matrix equations (size 2 x 2) in the form [**A][I]** = **V** for the circuit shown in Figure 2. Your final answer should contains numbers only in the **A** matrix and the **V** column vector.

(b) Using the result in part (a) solve the voltage *v* across the 4 Ω resistor.

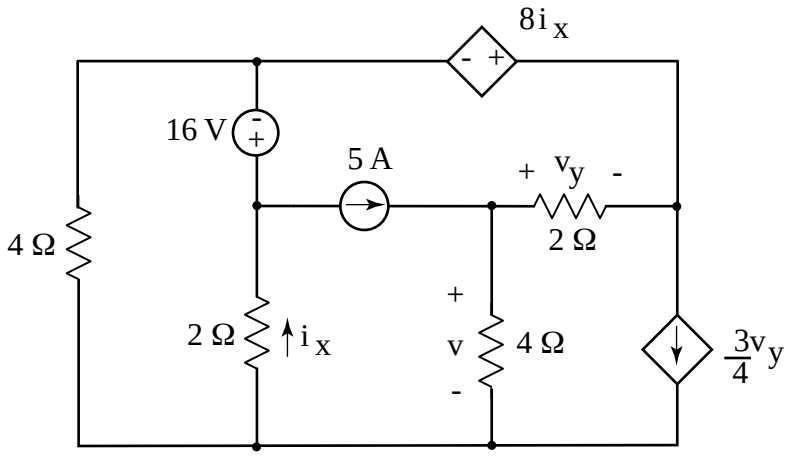


Figure 2

Q.3 (a) Using any method of your choice determine the steady state current $i_{out}(t)$ in the circuit shown in Figure 3 if $v_s(t) = 12\cos(2t + 45^\circ)$ V.

(b) Determine the natural response of this circuit assuming the capacitor held an initial voltage of $v_c(0^-) = V_0$ and the initial current through the inductor $i_L(0^-) = I_0$, respectively.

(c) If $I_o = -1A$ and $V_o = 2V$, plot $i_{out}(t)$ versus time.

(d) Plot the asymptotic frequency response of this circuit if i_{out} is considered the output of the circuit and the independent source as the input.

(e) If i_{out} is considered the output of the circuit and the independent source as the input, is this circuit reciprocal? Give a brief explanation for your reasoning.

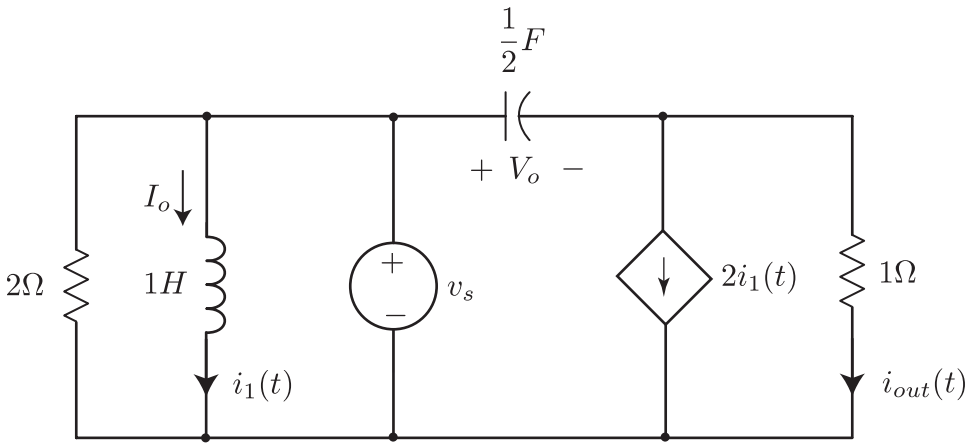


Figure 3

TOPIC: Digital Ciruits (ENCM467)

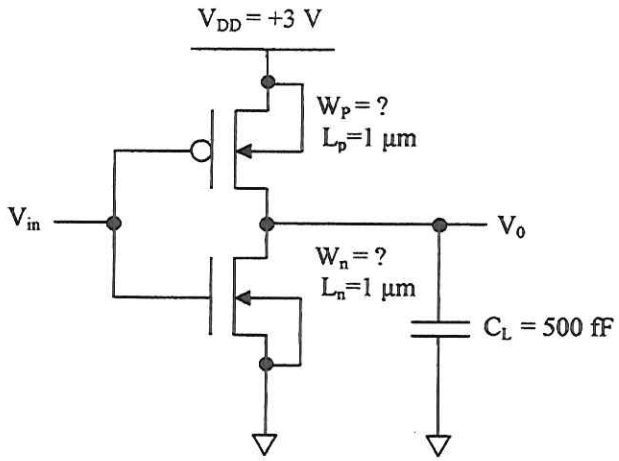
Q.1 Design a static CMOS inverter (see figure 2), using 1μm long nMOS and pMOS transistors and of appropriate widths, so as to meets the following performance requirements:

1) A falling delay of 0.2 ns, for an output transition from 2 V to 0.6 V, assuming an output load capacitance of 500 fF and ideal step input of 3V being applied to the inverter.
2) An inverter switching threshold voltage $V_{INV} = 1.4\,\text{V}$.

2μm CMOS device and process parameters

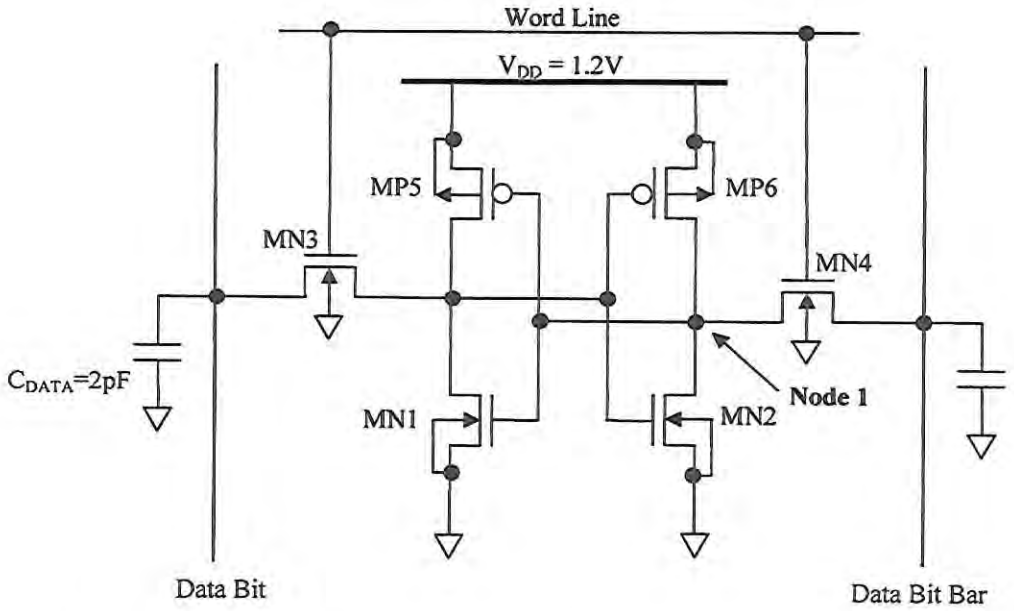
$k_n' = 100\ \mu\text{A.V}^{-2};\ V_{T0(n)} = 0.8\,\text{V};\ L_n = 1\,\mu m\ ;W_{n(\min)} = 2\,\mu m\ ;\ \gamma_n = 0.4\ \text{V}^{0.5};\ |2\phi_{F(n)}| = 0.6\,\text{V}$

$k_p' = 50\ \mu\text{A.V}^{-2};\ V_{T0(p)} = -1.0\,\text{V};\ L_p = 1\,\mu m\ ;W_{p(\min)} = 2\,\mu m;\ \gamma_p = 0.4\ \text{V}^{0.5};\ |2\phi_{F(p)}| = 0.6\,\text{V}$



Q.2 What are the respective widths of transistors MN4 and MP6 of the CMOS static memory cell shown below, so that the design meets the following requirements:

(a) The voltage at **node 1** during the **WRITE '1'** operation must be pulled down to at least **0.4 V.**

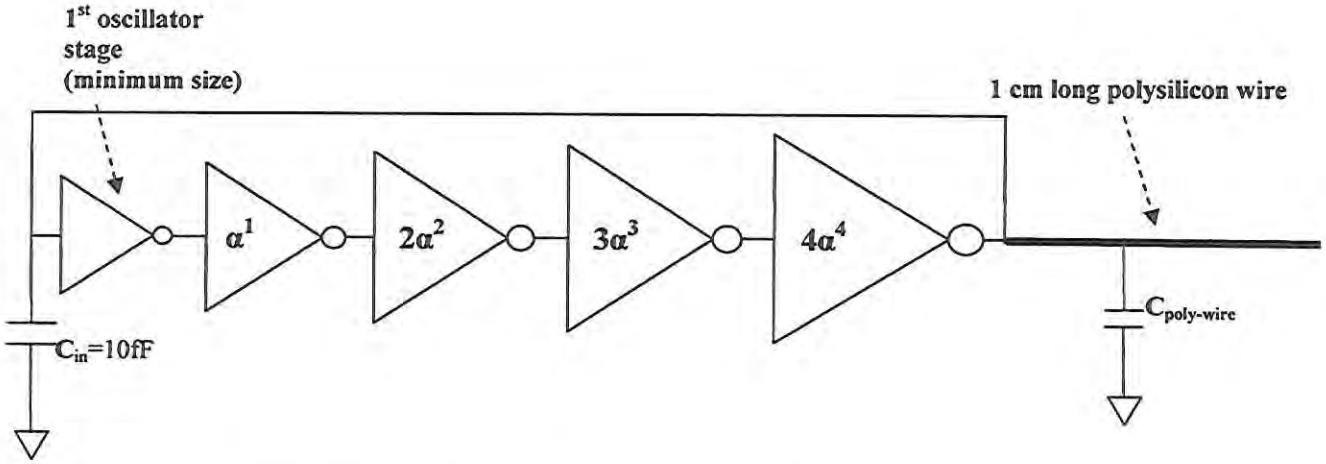


$k_p' = 130\ \mu A.V^2$; $k_n' = 400\ \mu A.V^2$; $V_{T0(n)} = 0.4\ V$; $V_{T0(p)} = -0.4\ V$; $\gamma_n = 0.2V^{1/2}$; $\gamma_p = 0.2V^{1/2}$
$|2\phi_F| = 0.88V$; $L_{MN1} = L_{MN2} = L_{MN3} = L_{MN4} = L_{MP5} = L_{MP6} = 0.1\mu m$;

Q.3 In order to generate an on-chip clock, a tapered a five stage ring oscillator is used in order to drive a long capacitive polysilicon wire, as shown below. The first ring oscillator stage is a minimum sized inverter with C_{in} = 10fF, and a propagation delay of 175 pS, when driving a similar minimum sized inverter. The sizes of the 2nd and subsequent stages are scaled by α, $2\alpha^2$, $3\alpha^3$, $4\alpha^4$ respectively. Given that that polysilicon line width is 5μm with a per unit area capacitance of 0.05 fF/μm^2

a). Determine the optimum scaling factor (α) of the ring oscillator stages in order minimize the propagation delay.

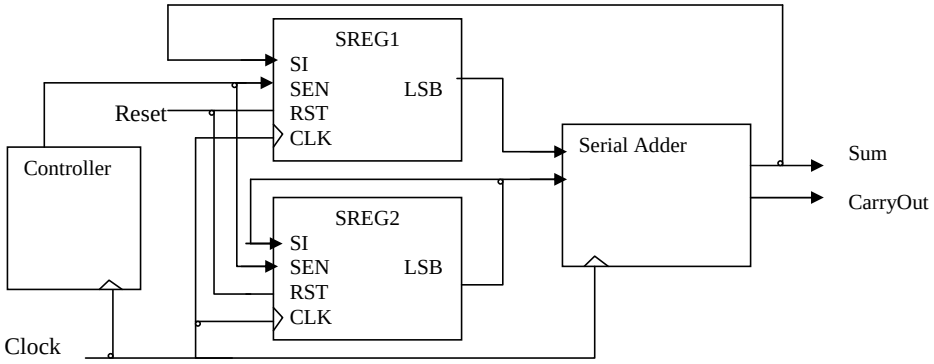
b). What is the frequency of oscillation of the tapered ring oscillator?



A 5 stage tapered ring oscillator driving a polysilicon wire

Q.1 (parts a-c on following pages)

Consider the serial adder below. Two shift registers $SREG1$ and $SREG2$ are used to hold the four bit numbers to be added. Each register has a Shift Enable signal SEN, serial input SI, Clock and Reset. When $SEN = 1$ and the Clock is pulsed, SI is entered into the Most significant bit, MSB, of the register, as the contents of the register are shifted right one position. The connections needed for initial loading of the registers are not shown. The upper register serves as accumulator, and after four shifts its contents is replaced with the sum of the initial numbers. The lower register is connected as a cyclic shift registers, so after four shifts it is back to its original state and the second number is not lost.



(a) [Design the Serial Adder block for the circuit above. It should include a full adder and a flip-flop to store carry, to be used at the next clock cycle. At each clock cycle, one pair of bits is added in the full adder. It should also include a logic which must accommodate the following operation involving Clock and the SEN signal: when SEN is 1, the carry bit is stored in the carry flip-flop on the clock edge.

(b) Design the Controller (based on a Mealy FSM) so that after receiving a start signal, N, it will output $SEN = 1$ for four clocks and then stop. $SEN = 1$ shifts the sum bit into the upper register and causes the lower register to rotate right. Draw the state graph and the state table. Assume that the start signal N is terminated before the network returns to the first state, so no further action occurs until another start signal is received. Once the second state is reached, the network operation continues regardless of the value of N.

(c) Provide an alternative high-level FSM for the FSM in part (b).

Q.2 (parts a-d on this and following pages)

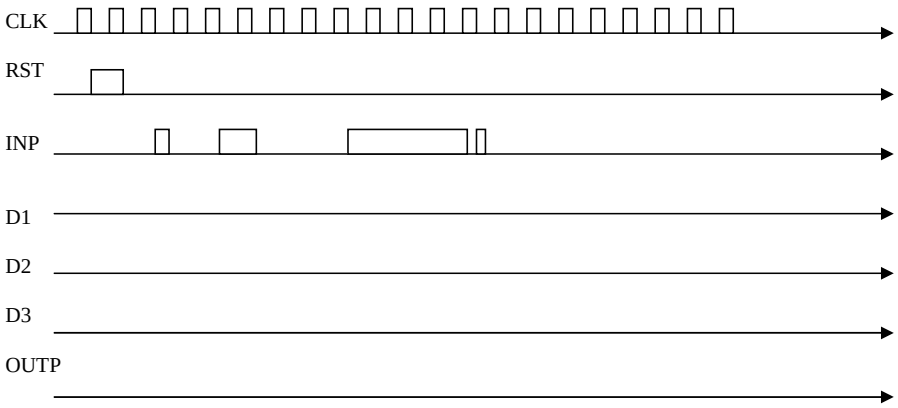
Consider the VHDL code that defines a debounce circuit, which can be used to qualify the input of a push-button switch.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity DEBOUNCE is
    port(INP, RST, CLK: in std_logic;
         OUTP: out std_logic;
end entity DEBOUNCE;

architecture BEHAV of DEBOUNCE is
 signal D1, D2, D3:  std_logic;
 begin
  process (CLK, RST)
  begin
    if (RST = '1') then
       D1 <= '0';
      D2 <= '0';
      D3 <= '0';
    elsif (CLK'event and CLK = '1') then
      D1 <= INP;
      D2 <= D1;
      D3 <= D2;);
     end if;
  end process;
      OUTP <= D1 and D2 and (not D3);
end architecture BEHAV;
```

(a) Draw the circuit and its timing diagram (see the template below) to answer the question: why this circuit is called a debounce circuit?



(b) In addition, the circuit ensures that the output indicating the button press is of fixed duration regardless of how long the actual button is pressed. How long is this fixed duration?

(c) Propose an alternative debounce circuit solution, based on a counter (draw the design schematics). Specify the counter size.

(d) Provide the VHDL fragment corresponding to the debouncer based on the counter from part (c) in the space provided below.

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_arith.all;

entity DEBOUNCE1 is
    port


end entity DEBOUNCE1;
architecture BEHAV of DEBOUNCE1 is









end architecture BEHAV;
```